The Design of CMOS Transimpedance Amplifier Based on BSIM Large-signal Model

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Abstract -- A modified BSIM CMOS RF large-signal model is presented for RF circuit design. The high-frequency CMOS model is based on BSIM3v3, by adding some passive components to describe the microwave behaviors. Integrated CMOS transimpedance (TZ) amplifier circuits were designed and fabricated base on this model. A 0.35 μm CMOS technology was used for circuit realization, and a capacitive-peaking [1-3] design to improve the bandwidth of TZ amplifier was also proposed and investigated .

I. INTRODUCTION

In an optical communication system, optoelectronic receivers which consists of a photodetector and a transimpedance amplifier, is used to convert the optical signals into electrical signals in the front end. Fig. 1 shows the system block diagram of optical fiber communication. A high gain and high speed transimpedance (TZ) amplifier plays a key component in the design of optoelectronic integrated circuits to amplify the input weak photo-currents into voltage signals. In the past, GaAs based devices such as MESFET, PHEMT and HBT are the most widely used technologies to implement the TZ amplifier circuits for high speed data rate operation [4-5]. However, as to the advanced performance progress in deep sub-micron CMOS technology, CMOS becomes a promising option to realize high-speed and high-frequency integrated circuits.

In this report, we used the developed modified non-linear BSIM3v3 model to design and fabricate a transimpedance amplifier based on 0.35 μm CMOS technology. The BSIM3v3 model is a physical-based model for deep sub-micron MOSFETs, which is commonly used in digital and analog circuit designs. As to the TZ amplifier design itself, a feedback topology is adopted to design a high gain TZ amplifier. In addition to the conventional TZ design, we also introduced a peaking technique in TZ amplifier design to improve it's bandwidth, where a shunt-capacitor peaking was used.

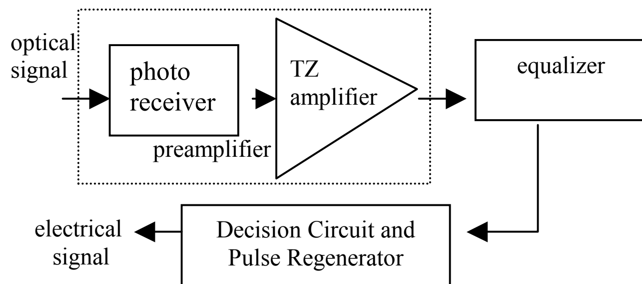

Fig. 1 Block diagram of optical fiber communication system

II. CMOS RF LARGE-SIGNAL MODEL

In a typical n-MOSFET device cross-section, the n^+-doped drain and source regions form a P-N junction inside the p-type substrates. It results in a series capacitance-resistance pair in the P-N junction depletion region. However, this substrate network is not included in a standard BSIM3v3 model, which will have a direct impact on RF power loss in substrates. This modified equivalent circuit model of MOSFET is shown in Fig. 2. The core device, M_1, represents the original BSIM3v3 model, and other passive components represent the high frequency parasitic effects according to MOSFET physical layouts. The parameters of BSIM3v3 and the added parasitic components are extracted by fitting device DC I-V characteristics and measured S-parameters up to 20 GHz.

The MOSFETs were fabricated by TSMC (Taiwan Semiconductor Manufacture Company) 0.35 μm 1P4M CMOS process. A multi-finger structure is used for RF applications. Each device's finger width is 5 μm. To establish a scaleable MOSFET RF large-signal model, devices with 50 μm, 80 μm, 100 μm and 200 μm, gate-width were characterized.

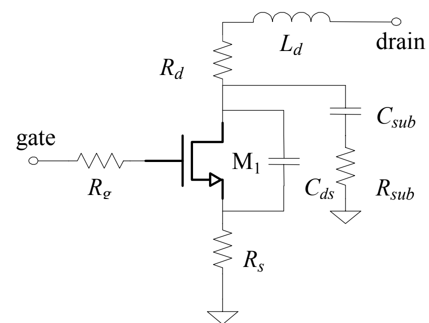

Fig. 2 The equivalent circuit model of MOSFET

Inherently, BSIM3v3 is a scaleable model within a limited gate-width and length dimension. It means different dimension MOSFET has the same BSIM3v3 model parameters. The added passive components are basically proportional to device dimension. In Fig. 2, R_g is the gate resistance of MOSFET RF large-signal model, and it can be scaled by the number of total gate finger (*m*). The C_{sub} and R_{sub} represents the substrate capacitance-resistance parasitic pair, which is formed by the depletion region between n^+-doped drain and p-type substrate. The parasitic effects at source terminal are negligible, because the source terminal is connected to p-type substrate and grounded during the measurement. Hence, C_{sub} and R_{sub} are scalable versus the P-N junction depletion region area, which is also a linear

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function of m. In the mean while, R_{sub} is related to silicon substrate impedance, which is inversely proportional to m, i.e. $R_{sub}=R_{sub0} / m$. The R_{sub0} is also the normalized substrate resistance. The C_{ds} in Fig. 2 represents the capacitance along the source to drain terminals. It is determined by the area of source/drain interconnection overlap region. This parameter can also be written as a linear function of m. The other resistances, R_s and R_d, represent the contact resistance from source and drain, respectively, which can also be linearly scaled by the number of drain and source area. The L_d is the series parasitic inductance in drain metal connection, which is an important parameter to fit the S-parameters up to 20 GHz. L_d is also associated with device physical dimension. Therefore, R_s, R_d and L_d are inversely proportional to gate-fingers (m). With each gate-width of 5 µm, the above parasitic components of MOSFETs for different gate-width can be simply linearly scaled by the finger numbers.

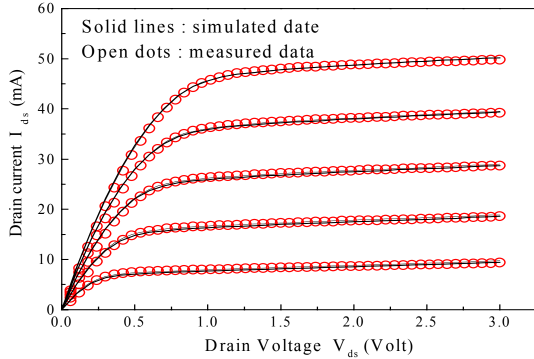

Fig. 3. The DC I-V measurement and fitting results with a gate width of 200 µm. (solid lines: simulation data, open points: measurement data) V_{ds} from 0V to 3V and V_{gs} from 1V to 2V, step 0.25V

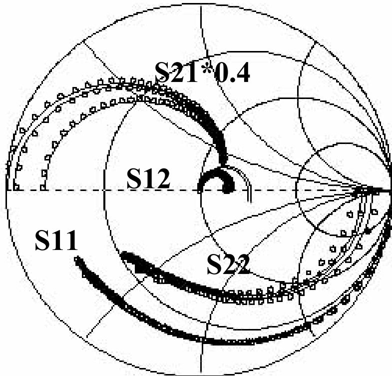

Fig. 4. The measurement and fitting results of S-parameters under various bias points from 50 MHz to 20 GHz, with a gate-width of 200 µm. V_{ds} = 3V, V_{gs} from 1V to 3V. (open circle points: measurement results, solid lines: simulation results)

0.35 µm gate-length MOSFETs with gate-width of 50 µm, 80 µm, 100 µm and 200 µm were fabricated and characterized to build up this scalable large-signal BSIM3v3 RF model. The peak transconductance (g_m), f_t and f_{max} biased at V_{ds} = 3 V, V_{gs} = 2 V are 200 mS/mm, 30 GHz and 30 GHz, respectively. By fitting the measured DC and RF data, those parasitic elements specified in Fig. 2 can be extracted individually. However, the parameters inside the BSIM3v3 model remain fixed during the fitting procedure. Fig. 3 and Fig. 4 show the device I-V and microwave S-parameter characteristics (up to 20 GHz) for MOSFETs with a gate-width of 200µm. The fitting results are also included in these figures, and the extracted parasitic elements can therefore be obtained, which concludes the finalization of this scalable CMOS non-linear BSIM model[6].

III. CMOS TZ AMPLIFIER CIRCUIT DESIGN

The TZ amplifier has demonstrated to be the most suitable solution used as a preamplifier for optical receiver front-end circuits. The TZ amplifiers present the advantages of simplicy, high bandwidth and large dynamic range as shown in Fig. 1. Although many published reports proposed the designs of CMOS TZ amplifier for GHz bandwidth performance; however only few papers demonstrated experimental results in achieving GHz bandwidth, but with complicated circuit structures. In this report, a simple TZ structure was designed for a gigahertz bandwidth operation. The schematic of the TZ amplifier is shown in Fig. 5, which is based on a shunt-shunt feedback circuit topology. It includes a common source gain stage, a resistive feedback loop (R_f) and two output matching buffer stage. The amplifier transfer function can be written as

$$T = \frac{\alpha(s)}{1+\alpha(s)\beta(s)} \qquad \beta(s) = -\frac{1+sR_fC_f}{R_f} \qquad (1)$$

where α(s) is the open loop transfer function and β(s) is the feedback transfer function.

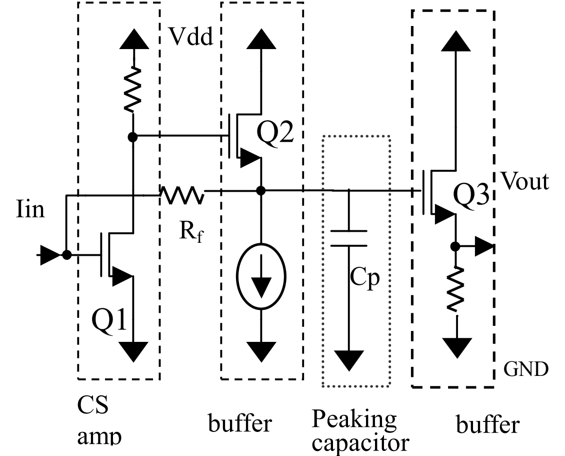

Fig. 5 Schematic of TZ amplifier with a peaking capacitor

Since R_f is the feedback resistance, by varying the value of R_f one can adjust an appropriate gain and bandwidth. C_f is the parasitic capacitor associated with R_f. For further enhancing the operational bandwidth, a shunt peaking-capacitor (C_p) is added in Fig. 5.

The open loop transfer function α(s) of conventional TZ amplifier is give by equation (2); while by adding a peaking capacitor it creates an extra pole in original TZ design, which is expressed in equation (3).

$$\alpha(s) = \frac{A}{1+\frac{s}{\omega_1}} \qquad (2) \qquad \alpha_{Cp}(s) = \frac{A}{(1+\frac{s}{\omega_1})(1+\frac{s}{\omega_2})} \qquad (3)$$

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A is the low-frequency open loop gain of the TZ amplifier. The ω_1 is caused by the total input capacitance, and the ω_2 shown in equation (3) is the extra pole resulting from the added Cp. The close loop transfer function of the TZ amplifier before (T) and after adding (T_{Cp}) a peaking capacitor is given by

$$T = \frac{-AR_f}{(A-R_f)+s(AR_fC_f-\frac{R_f}{\omega_1})} = \frac{T(0)}{1+\frac{s}{\omega_{3dB}}} \qquad (4)$$

$$T_{Cp} = \frac{\frac{A\omega_1\omega_2}{(s+\omega_1)(s+\omega_2)}}{1-\left[\frac{A\omega_1\omega_2}{(s+\omega_1)(s+\omega_2)}\right]\cdot\left(\frac{1+sR_fC_f}{R_f}\right)} = \frac{A\omega_1\omega_2}{s^2+s\frac{\omega_0}{Q}+\omega_0^2} \qquad (5)$$

Equation (4) can be expressed with a dominate pole $\omega_{3dB} \approx (1+A\beta)\omega_1$ and T(0) is the low-frequency TZ gain. However, ω_0 is the pole frequency in equation (5). For Q factor >0.5, the poles of equation (5) are complex conjugate. If Q equals 0.707, it results in a maximum frequency response (butterworth design), and peaking effect occurs when Q is greater than 0.707. Based on this concept one may simply varies the values of Q by controlling the peaking capacitance Cp to adjust the bandwidth of the TZ amplifier without sacrificing its low-frequency transimpedance gain. The final layout of CMOS TZ amplifier with a capacitor-peaking is shown in Fig. 6, where 50 and 200 µm-wide gate nMOS were used (Q1 and Q3 : 50 µm-wide; Q2 : 200 µm-wide). Peaking capacitance is 1pF in our design to achieve the condition of Q = 0.707.

IV. CHARACTERISTICS OF CMOS TZ AMPLIFIER WITH A CAPACITIVE-PEAKING

HP ADS simulator was used to establish the CMOS large signal model and evaluate the performance of CMOS TZ amplifiers. Fig. 7 shows the simulated and measured DC characteristics. Notice that by adjusting the input current from 0 µA to 50 µA, output voltages gradually move from 778mV to 752mV, and the associated measured DC gain is 501 Ohm, which corresponds to a transimpedance gain of 54dB. However, the DC gain slightly decreases in the high current injection region. By adding a shunt peaking-capacitor (1pF) in Fig.5, the simulated 3dB bandwidth was enhanced from 960 MHz to 1.3 GHz, which is shown in Fig. 8 (a). As to the measured frequency response evaluated by network analyzer demonstrated an improved 3dB bandwidth from 875 MHz to 1.35 GHz, which is shown in

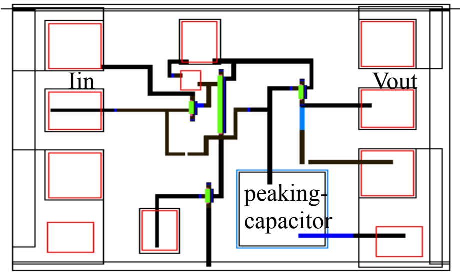


Fig. 6 Layout of the TZ amplifier with a C-peaking design

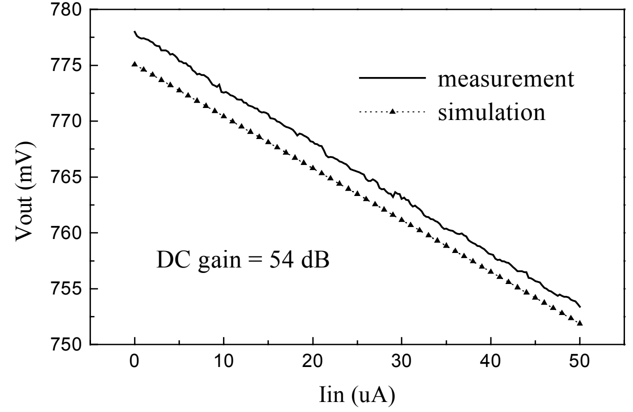
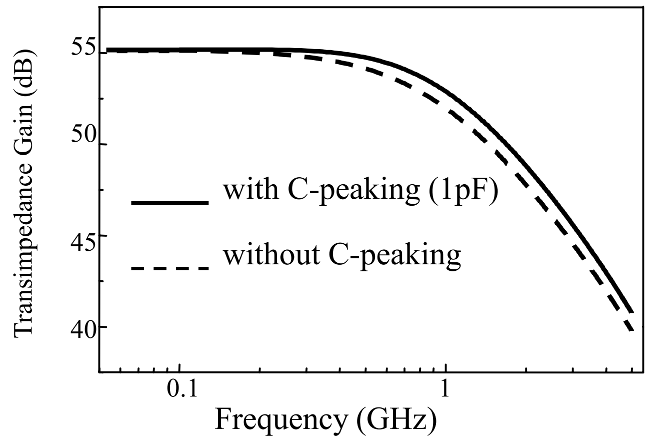


Fig. 7 Measured DC gain of CMOS TZ amplifier



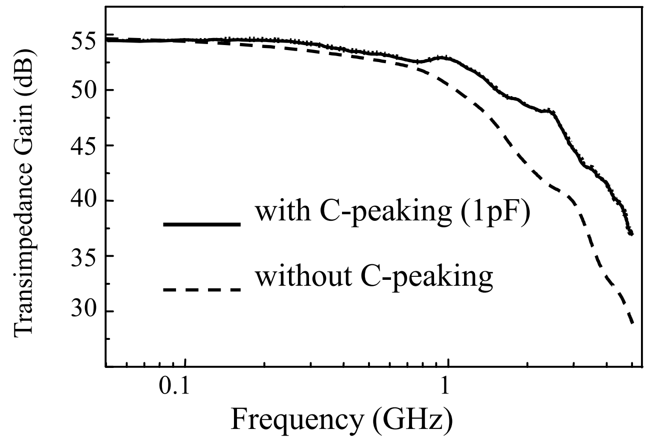


Fig. 8 (a)Simulated frequency response of CMOS TZ amplifier with and w/o C-peaking
(b)Measured frequency response of CMOS TZ amplifier with and w/o C-peaking

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Fig. 8 (b), by a factor of 54 %. The low-frequency transimpedance gain of both simulated and measured is 54 dB, which corresponds quite well with the BSIM model predictions. A slight bandwidth difference of simulation and measurement data may be caused by the insufficient resistor models required.

By using ESG (digital signal generator), a 2^9-1 pseudorandom bit sequence (PRBS) at 1.2Mbps was carried by microwave signals with an 0dBm power. After the FSK modulation, the signal was injected into the input of CMOS TZ amplifiers, and output eye diagram was measured by an HP89441 (vector signal analyzer). Clearly, opened eye diagrams (shows in Fig. 9) were obtained, and demodulated FSK error increases from 1.08 % rms to 1.88 % rms as the carrier frequency increases from 0.5GHz to 2.65GHz, shown in Fig. 10.

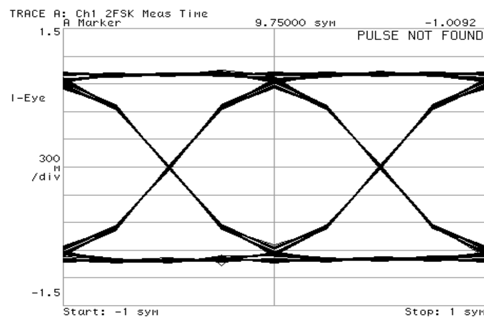

Fig. 9 Eye diagram of the TZ amplifier at 1.2Mbps (carrier freq = 2.65GHz)

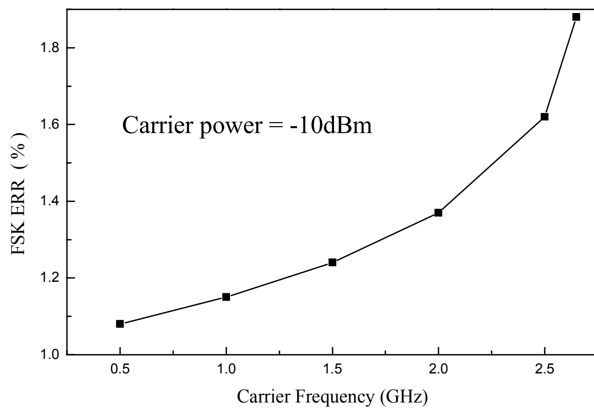

Fig. 10 Demodulated FSK error at output of CMOS TZ amplifier

V. CONCLUSIONS

In summary, a scaleable 0.35 µm MOSFET RF large-signal model is presented covering different gate-width, based on BSIM3v3 model. It can predict the device characteristics up to 20 GHz under various biasing conditions. Using these models, a CMOS TZ amplifier circuit design for a GHz operation was presented. Base on a capacitive peaking technology , the 3dB bandwidth is enhanced from 875MHz to 1.35 GHz without sacrificing its low-frequency gain. This method provides an easy way to improve the bandwidth of TZ amplifier and enhance the performance of receiving circuit in optical communication systems.

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